WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY
(SUPPLEMENTARY SHEET)
International File No. PCT/DE2004/001622

Re.: Point V

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Reference is made to the following document(s):

   D1: US 5 107 245 A (BECKER AUTORADIOWERK), 21 April 1992*

   * relates to a document that verifies the general technical knowledge of those skilled in the art.

2. The combined object of Claims 1 and 2 does not fulfill the requirements of Article 33(3) PCT in regard to inventive step.

2.1. The object of these claims is interpreted to mean that when an erroneous behavior of the timing generator is detected, this event is first stored asynchronously by setting a bit in a (second) memory element, and that when the clock is again working reliably this bit is transferred to a (first) memory module which requires the clock pulse (see objections regarding clarity under Point VIII, Section 1).

2.2. Document D1 (see in particular Figure 1 and the corresponding text) describes a control unit (monitoring circuit 22 with drive circuit 40 and evaluating circuit

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46) having an oscillator (16) for a processor (microcomputer 14) for detecting and indicating absences of oscillation in an automobile, the stability of the timing generator in automobiles being recognized as essential for the correct functioning of the electronics (column 1, lines 56 to 59), so that the mere recognition of this problem cannot contribute to an inventive step.

As is well known to those skilled in the art maintenance services, specifically for automobiles, are performed at certain time or mileage intervals, it being customary to store (better known under the term "log") information (such as exhaust values, fuel consumption or errors that have occurred in the interim) in memory modules in order to make the analysis significantly easier for the service personnel.

Since, as is also well known to those skilled in the art, the timing generator is a critical element which is central to the functioning of the electronics in electronics of every type (and particularly so in automobiles, as revealed in D1), those skilled in the art would therefore also store an erroneous behavior of the timing generator, and at the same time would naturally immediately recognize that as long as the clock is not reliable or is not oscillating at all this can only be done asynchronously (or with the aid of a fall-back clock, as in D1). If he then considers it necessary, he can transfer this asynchronously stored error (synchronously) when the clock resumes into a memory that requires a clock (see also objections under Point VIII, Section 3).

2.3. Starting from D1 and using only general technical knowledge, one would thus arrive at the combined object of Claims 1 and 2, which is therefore obvious.

3. Subordinate Claims 2 through 5 contain no features which, in combination with the features of any claim to which they refer, fulfill the requirements of the PCT in regard to inventive step.

3.1. As for Claim 3, aside from asynchronously setting a memory bit when the clock signal is absent, which is obvious for the reasons set out in Section 2, it contains merely the well-known start-up time or transient phase the first time the supply voltage is applied.

3.2. The additional features of Claims 4 and 5 relate to the well-known resetting of memory elements.

4. For the reasons stated in Sections 3 and 4, the present Claims 1 through 5 cannot be granted. In view of the available related art, it is also not possible to recognize that part of the application could form the basis of a new, grantable claim. It must therefore be expected that a negative IPER will be issued.

In Reference to Point VII

Certain defects in the international application

1. Contrary to the requirements of Rule 5.1(a)(ii) PCT, document D1 is not named in the description, and its relevant content is not at least briefly outlined.

2. Contrary to the requirements of Rule 6.3(b) PCT, independent Claim 1 is not composed in the two-part form - appropriate in the present case - in which features which are known in combination from the related art (see

D1) are included in the definition of the species of the claim (Rule 6.3(b)(i) PCT), and the other features are included in the characterizing part of the claim (Rule 6.3(b)(ii) PCT).

In Reference to Point VIII

Certain remarks on the international application

1. In Claim 1 it is not clear how the event of an (only) temporarily interrupted clock pulse is able to be stored in a first error memory (which requires a clock pulse), if the clock pulse needed for writing the error memory is not present. To that end it is necessary, at the moment of the interruption, to record this event asynchronously in a different memory element (see page 2, lines 5 to 20, and page 4, line 17 to page 5, line 21 and Figure 1). Since this feature, which is contained only in Claim 2, is essential to solving the problem according to the present invention, it should be included in independent Claim 1.

2. It is stated in Claim 2 that the event of the absence of oscillation of the timing generator is stored in a (second) error memory, without specifying that this memory must necessarily be an asynchronous memory (entirely the opposite of the first error memory, which is not written to until a clock signal begins again); this is however immediately clear to those skilled in the art, even if this is not revealed in the description.

3. Claims 1 and 2 refer to a first and a second error memory, the bit which is set in the second error memory when oscillation of the timing generator is interrupted being transferred to the first error memory when oscillation begins, without the description giving a

reason for this redundant storing. A reason immediately evident to a person skilled in the art would be the recording of vehicle data over a certain time period, which is widespread primarily in automobiles, although this is not evident from the description (page 5, lines 11 to 15). This redundant storage therefore represents a redundant measure, which has no particular technical effect.

4. Claims 2 through 5 refer to a second error memory, which is set when oscillation of the oscillator is interrupted (necessarily asynchronously; see objections in Section 2 above) and is reset when oscillation of the oscillator begins again, the description referring consistently to a non-volatile memory, namely an EEPROM (see e.g. page 2, lines 10 to 12 or page 4, lines 34 and 35; also see Figure 1), without revealing the reason for this special type of memory. The only thing essential to the invention first of all is that this bit is settable and resettable asynchronously (see objections under Section 2), which is achieved in the simplest case by the widely known SR latch. But at the same time it is immediately clear to those skilled in the art that oscillation interruptions which do not begin again before the engine and hence the battery are turned off would not be recognized, since the volatile SR latch loses its memory state when the supply voltage is shut off, and it would therefore naturally employ a non-volatile memory module.

5. Claim 3 refers to a timer module which ensures that the clock signal which is still not present after a certain on-time is stored as an error in the (asynchronous) second error memory, it being immediately clear to a person skilled in the art, even if not revealed in the description, that this must be an analogous module (and

not a digital synchronous standard timer module, which of course can only count when a clock signal is present).

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